Day 1 Tuesday, May 19, 2026 *Technical Breakout Sessions (each session is 35 mins presentation/Q&A + 10mins break/transit time)*

Time / Room	Palomino 6 (130) AI	Palomino 7 (130) AI/HPD	Palomino 8 (100) HPD	Palomino 9(100) TM/SiPho/RF	Palomino 10 (100) RF	Moor2 (40) HT/TM	Moor3 (40) TM	Bourbon 11 (30) T2000/FA
8:00 AM	WELCOME AND EVENT HIGHLIGHTS AND KEYNOTE 1							
11:10 AM	**11 - Artificial Intelligence** AI-Driven Automation System for V93000 ATE	**168 - Artificial Intelligence** Bridging Fragmented Expertise: An On-Premises Retrieval Platform for Test Engineers	**48 - High Performance Digital** Taming the Demand for Digital Instruments for Rising Pin Counts of HPC Testing Applications	**170 - Silicon Photonics** PICs Wafer-Level Testing Using Dynamic Optical Alignment	**36 - RF** Best Practice of Bluetooth Channel Sounding Test on V93000	**83 - Hot Topics** Preventing Thermal Runaway with Advanced Monitoring Solutions	**164 - Test Methodologies** Dynamic In-Memory Test Pattern Modification Techniques for Efficient Test on High-Security Devices	**10 - T2000** High-Efficiency, High-Volume Measurement of Basic Electrical Characteristics of MEMS Using the T2000
11:55 AM	**12 - Artificial Intelligence** V93000 AI-Driven Test Program Development: Flexible Integration of Cutting-Edge Generative AI Technologies	**196 - Artificial Intelligence** Innovative HSIO Tx Termination Calibration Using a Supervised Machine Learning Approach	**53 - High Performance Digital** Using Interleaved Testflow Execution on Heterogeneous Dies for HPC Chips	**210 - Silicon Photonics** Wafer-Level HVM PIC Testing Using V93000-Triton Photonics Solution	**138 - RF** Automated RF Power De-embedding via Handler-Based Site-by-Site Calibration for SoC Mass Testing	**121 - Hot Topics** New DC Profiling Methodology for Optimized Performance	**16 - Test Methodologies** A Scalable Multi-Die Test Solution for Large-Scale AI Chip Production	**25 - T2000** A New Approach to Real-Time Large-Volume Data Transfer in Semiconductor Test Systems
12:40 PM	LUNCH & EXPO							
2:00 PM	**50 - Artificial Intelligence** Scaling LLM Intelligence in Semiconductor Test with MCP Servers and Multi-Agent Architectures	**181 - Artificial Intelligence** From NLP to ATE: Model-Free Search Optimization Using FAISS and ACS	**41 - High Performance Digital** Interleaved Test Flow for Chiplet Testing	**140 - Silicon Photonics** HVM Photonics Testing Solution Using Die-Level Prober (DTS-650) and V93000	**225 - RF** An Overview of Next-Generation UWB (IEEE 802.15.4ab): Applications and Test Challenges	**21 - Test Methodologies** Dynamic Debug Tool	**175 - Test Methodologies** Efficient On-Die Current Meter Calibration Leveraging XPS and Adaptive Testing	**28 - T2000** PMIC 3-Minute PGM Setup on T2000: One-Click APG Boosts Throughput
2:45 PM	**222 - Artificial Intelligence** Intelligent Probe Pin Defect Analysis: FastSAM-Based Image Extraction and AI-Driven Classification	**9 - Test Methodologies** SSN and IJTAG-Aware ATE: New Features in SmarTest and Tessent Shell for Efficient SSN and IJTAG Integration	**186 - High Performance Digital** MIPI C-PHY 3-Level Signal Driver Low-Cost Solution with PS5000 on EXA Scale	**224 - Silicon Photonics** Enabling HVM Test of Co-Packaged Copper and Optical Devices: Modular Platform Approach	**57 - RF** Extending RF Measurement Performance with Dual Measurement Capability in WSRF20ex	**203 - Test Methodologies** Comprehensive eFuse Burning Process Integrated Solution Based on ATE	**192 - Test Methodologies** Debugging Devices Under Test at Firmware Level with OpenOCD and Pin Scale 5000 Protocol Link	**115 - T2000** Noise Effects in Low Voltage, High Dynamic Range Devices and Test System Design
3:30 PM	BREAK & EXPO							
3:50 PM	**113 - Artificial Intelligence** Enhancing Test Code Quality with AI: Automated Unit Test Generation By Using GitHub Copilot and Smart-CI	**165 - Test Methodologies** Effective Scan Failure Analysis Utilizing SSN Pattern Isolation Test Method Using SmarTest 8	**109 - High Performance Digital** Fast Single-Shot Jitter Measurement in Production Test Using a PSMLS Card's Digitizer	**46 - APAM** Best Practices for Migrating APBB Applications from SMT7 to SMT8 on V93000 EXA Scale	**60 - RF** Best Practice of UWB Production Testing on V93000	**52 - Test Methodologies** ATE Machine Learning Optimized Vmin Search	**197 - Test Methodologies** HSIO Calibration and DC Measurement: Driving Accuracy for Reliable Test Solutions	**159 - T2000** T2000 Utility Tools and Libraries for Faster and More Efficient Test Program Development
4:35 PM	**51 - Artificial Intelligence** Accelerated Case Study: Successfully Migrating a CPU Project from SmarTest 7 to 8 with GitHub Copilot	**92 - High Performance Digital** A Real Case Study on Testing Customized AI Devices Using IMR and Intra-Site Memory Sharing on SmarTest 8	**71 - High Performance Digital** Test Scheme for DDR Clock Driver Chip Based on Pin Scale Multilevel Serial	**1 - APAM** An Important Research for High-Speed and High-Performance ADC HVM on the V93000 Platform	**5 - RF** A New Practical Solution to Improve the Phase Noise Performance of the Measure Receiver with WSRF20ex	**102 - Test Methodologies** AI-Assisted Offline Verification Solution for Reliable SmarTest 8 Test Programs	**202 - Test Methodologies** Custom SmarTest 8 SmarTest Work Center Eclipse Plug-In Development Using the Device Debug API	**123 - T2000** New BOST Solution for High-Speed Interface Testing in Next-Generation Display Driver ICs
5:20 PM	HAPPY HOUR & EXPO							

Day 2 **Wednesday**, May 20, 2026 *Technical Breakout Sessions (each session is 35 mins presentation/Q&A + 10mins break/transit time)*

Time / Room	Palomino 6 (130) AI	Palomino 7 (130) HPD	Palomino 8 (100) HPD	Palomino 9(100) APAM	Palomino 10 (100) RF	Moor2 (40) TM	Moor3 (40) TM	Bourbon 9(20) FA/TM/HSDI
8:00 AM	WELCOME, KEYNOTE 2 AND BREAK							
10:30 AM	**131 - Artificial Intelligence** Real-Time Anomaly Detection in ATE Using Deep Neural Networks on NVIDIA DGX Spark™	**180 - High Performance Digital** Power of Visualization — Maximizing EXA Scale Background Profiling	**111 - High Performance Digital** Test Time Reduction Using Interleaved Independent Testflow Executions	**3 - APAM** JESD204B/C High-Speed Protocol Solution with Pin Scale Multilevel Serial	**99 - RF** WSRF20ex Migration, Featuring Wi-Fi 7 Device and Test Time Reduction Through Site-Interlacing	**161 - Test Methodologies** Cost-Efficient Reliability in Wafer-Level Testing: Using CRES to Prevent Pin Degradation and Burn in Ganged XPS	**82 - Test Methodologies** Left-Shift First Silicon Bring-up: Emulated Validation of Structural Tests Over High-Speed IO	**35 - Factory Automation** ACS Data Feed Forward (DFF): A Unified Platform for Semiconductor Test Data Collection and Distributions
11:15 AM	**134 - Artificial Intelligence** Automated Machine Learning and Integration Framework for Scalable AI-Driven Test Optimization on the V93000	**6 - High Performance Digital** Analysis of a PCIe Signal Path Between the Root Complex and the Endpoint to Support Scan Tests	**125 - High Performance Digital** Leveraging Java's Multithreading Concept to Improve Test Program Loading Time	**49 - APAM** Best Practice of Deploying PMUX02 in PAC Project	**87 - RF** 20G High-Speed ADDA Device Testing from WSRF8 to WSRF20ex	**154 - Test Methodologies** An Efficient Algorithm for Time Measurement Unit (TMU) Data Filtering in Multisite Testing	**226 - Test Methodologies** Streamlined Read Patterns for Efficient Memory Use and Precise Failure Logging with SmarTest 8	**23 - Factory Automation** JSON Parser Tool for Automation of Offline Result Emulation (ORE) in SmarTest 8
12:00 PM	LUNCH & EXPO							
2:00 PM	**216 - Artificial Intelligence** Context is All You Need: Using Canonical Models and Multi-Agents to Automate Test Program Generation	**31 - High Performance Digital** Experience and Best Practices of Using PSMLS for DRAM Interface SoC (RCD/CKD) Testing on V93000	**169 - High Performance Digital** Advanced Thermal Profiling and Protection for Large HPC Devices in SmarTest 8	**91 - APAM** Test Solution for Automotive SBC-PMIC with Integrated DSI3 Interface	**143 - RF** Testing RF Devices with 14Gbps High-Speed Interface Using WSRF8 and PSMSL	**223 - Test Methodologies** Accelerating SoC Validation: From Rapid Bring-Up to Power-Performance Characterization	**205 - Test Methodologies** New Streaming Scan Network API-Based Library in SmarTest 8	**172 - HSDI** Innovative Test Hardware Design Strategies for the V93000's DUO Interface
2:45 PM	**153 - Artificial Intelligence** Adaptive Testing Techniques for Next-Generation Datacenter and AI Processors	**38 - High Performance Digital** Die-Level Testing, a New Test Insertion for High-Performance Digital	**147 - High Performance Digital** Speeding Up SSN Tests with the Result Per-Core (RPC) Feature	**162 - APAM** Comprehensive Test Coverage for Automotive Application Specific Standard Products: A Tester-Based Approach	**152 - RF** A High-Efficiency ATE Solution for Multi-Mode Satellite Terminal SoC Chips on V93000	**144 - Test Methodologies** Synchronized Execution - Safe Global Variable Usage in Background Threads with releaseTester() in SmarTest 8	**206 - Test Methodologies** Ensuring Integrity in OTP Programming During Production Testing	**218 - HSDI** Enhancing Test Program Performance by Leveraging Device Setup Metrics
3:30 PM	**158 - Artificial Intelligence** Decoupling Test and Processing with ACS-RTDI: An Inline Fuse Build Case	**74 - High Performance Digital** Rapid Power Sequence Simulation and Verification Solution in SmarTest 8	**132 - High Performance Digital** 1000A HPC Device Compatible LB Design on EXA scale	**104 - APAM** Leveraging XPS128+HV for Switch Charger Testing on EXA Scale	**184 - RF** Accurate and Efficient RF PA Digital Predistortion Calibration Using WSRF-8 Measurement		**150 - Test Methodologies** Enhanced Characteristic Test Solutions Based on New AI and SmarTest 8 Features	**96 - HSDI** An Integrated Solution for V93000 Test Program Quality Check and Analysis
4:15 PM	Break and Technology Kiosk Showcase							